Amendments to the Claims:

Prior to calculation of the filing fee, please cancel claims 2-26. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (original) A method for forming a MOS transistor having elevated source and drain structures, comprising:

providing a sacrificial gate pattern on a substrate;

providing an epitaxial layer on the substrate adjacent the sacrificial gate pattern;

providing a first insulating layer and a second insulating layer on the epitaxial layer adjacent the sacrificial gate pattern;

removing the sacrificial gate pattern to expose a portion of the substrate and wall portions of the epitaxial layer;

providing a gate dielectric layer on the exposed portion of the substrate and along the wall portions of the epitaxial layer;

providing a gate electrode on the gate dielectric layer;

removing the second insulating layer and the first insulating layer;

doping the epitaxial layer with impurities using the gate electrode as a mask to form source/drain extension regions in the epitaxial layer proximal to the gate dielectric layer;

providing insulating spacers on sidewalls of an upper portion of the gate electrode; and

doping the epitaxial layer with impurities using the gate electrode and insulating spacers as a mask to form deep source/drain regions adjacent the source/drain extension regions.

2-26 (canceled)

27. (original) A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at lower side portions of the gate electrode; and

insulating spacers on the epitaxial layer at an upper side portion of the gate electrode.

28. (original) The transistor of claim 27 wherein the gate dielectric layer extends across a bottom portion and the lower side portions of the gate electrode;

29. (original) The transistor of claim 27 wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

30. (original) The transistor of claim 27 further comprising second source/drain regions adjacent the first source/drain regions opposite the gate electrode .

31 (original) The transistor of claim 29 wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.

32. (original) The transistor of claim 29 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

33. (original) The transistor of claim 29 wherein the depth of the first source/drain regions is less than the depth of the second source/drain regions.

34. (original) The transistor of claim 29 wherein the second source/drain regions extend into a portion of the substrate.

35. (original) The transistor of claim 29 wherein the first source/drain regions extend into a portion of the substrate.

36. (original) The transistor of claim 27 wherein the substrate is formed of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

37. (original) The transistor of claim 27 wherein the epitaxial layer comprises silicon or silicon germanium.

38 (original) The transistor of claim 27 wherein the gate dielectric layer and gate electrode extend into a trench formed in an upper portion of the substrate.

39. (original) The transistor of claim 38 wherein the trench is of a depth that is less than 50nm.

40. (original) The transistor of claim 27 further comprising a channel region in the substrate under the gate electrode and adjacent the lower side portions of the gate electrode.

41. (original) The transistor of claim 27 wherein the gate dielectric layer comprises a material selected from the group of materials consisting of: silicon oxide film; silicon oxy-nitride (SiON); tantalum oxide; and a high-dielectric-constant material.

42. (original) The transistor of claim 27 wherein the gate dielectric layer is formed using a deposition or thermal oxidation process.

43. (original) The transistor of claim 27 wherein the gate electrode comprises a material selected from the group of materials consisting of polysilicon film; silicon geranium film; silicide film; metal film; and a laminate film.

44. (original) The transistor of claim 27 further comprising a silicon oxide buffer layer between the gate electrode and the insulating spacers.

45. (original) The transistor of claim 27 further comprising a silicide film on the source/drain regions and the gate electrode.

46. (original) The transistor of claim 45, wherein the silicide film comprises a material selected from a group consisting of Co, Ni, W, Ti and combinations thereof.

47. (original) A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode; and

second source/drain regions adjacent the first source/drain regions opposite the gate electrode.

48. (original) The transistor of claim 47 wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

49. (original) The transistor of claim 47 further comprising insulating spacers on the epitaxial layer at an upper side portion of the gate electrode, wherein the second source/drain regions are

formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.

50. (original) The transistor of claim 49 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

51. (original) The transistor of claim 47 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

52. (original) The transistor of claim 47 wherein the first source/drain regions are formed to a first depth in the epitaxial layer and wherein the second source/drain regions are formed to a second depth, wherein the first depth is less than the second depth.

53. (original) The transistor of claim 47 wherein the second source/drain regions extend into a portion of the substrate.

54. (original) A MOS transistor having elevated source and drain structures, comprising:

a substrate having a trench in an upper portion thereof;

a gate dielectric layer lining the trench;

a gate electrode on the gate dielectric layer, the gate electrode extending into the trench, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode; and

second source/drain regions adjacent the first source/drain regions opposite the gate electrode .

55. (original) The transistor of claim 54 wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

56. (original) The transistor of claim 54 further comprising insulating spacers on the epitaxial layer at an upper side portion of the gate electrode, wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.

57. (original) The transistor of claim 56 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

58. (original) The transistor of claim 54 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

59. (original) The transistor of claim 54 wherein the first source/drain regions are formed to a first depth in the epitaxial layer and wherein the second source/drain regions are formed to a second depth, wherein the first depth is less than the second depth.

60. (original) The transistor of claim 54 wherein the second source/drain regions extend into a portion of the substrate.

61. (original) The transistor of claim 54 wherein the first source/drain regions extend into a portion of the substrate.

62. (original) A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

source/drain extension regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode formed by doping the epitaxial layer with impurities;

insulating spacers on the epitaxial layer at an upper side portion of the gate electrode; and

deep source/drain regions adjacent the source/drain extension regions opposite the gate electrode, wherein the deep source/drain regions are formed by doping the epitaxial layer with impurities using the gate electrode and insulating spacers as a mask.

63. (original) The transistor of claim 62 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

64. (original) The transistor of claim 62 wherein the deep source/drain regions extend into the substrate under the epitaxial layer.

65. (original) The transistor of claim 62 wherein the source/drain extension regions extend into a portion of the substrate.

66. (original) The transistor of claim 62 wherein the gate electrode extends into a trench formed in an upper portion of the substrate.

67. (original) A MOS transistor having elevated source and drain structures, comprising:

a substrate having a trench in an upper portion thereof;

a gate dielectric layer lining the trench;

a gate electrode on the gate dielectric layer, the gate electrode extending into the trench, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

source/drain extension regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode formed by doping the epitaxial layer with impurities;

insulating spacers on the epitaxial layer at an upper side portion of the gate electrode; and

deep source/drain regions adjacent the source/drain extension regions opposite the gate electrode, wherein the deep source/drain regions are formed by doping the epitaxial layer with impurities using the gate electrode and insulating spacers as a mask.

68. (original) The transistor of claim 67 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

69. (original) The transistor of claim 67 wherein the deep source/drain regions extend into the substrate under the epitaxial layer.

70. (original) The transistor of claim 67 wherein the source/drain extension regions extend into the substrate under the epitaxial layer.

71. (original) The transistor of claim 67 wherein the trench is of a depth that is less than 50nm.

72. (original) A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate; and

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at lower side portions of the gate electrode.

73. (original) The transistor of claim 72 further comprising insulating spacers on the epitaxial layer at an upper side portion of the gate electrode.

74. (original) The transistor of claim 72 wherein the gate dielectric layer extends across a bottom portion and the lower side portions of the gate electrode;

75. (original) The transistor of claim 72 wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

76. (original) The transistor of claim 72 further comprising second source/drain regions adjacent the first source/drain regions opposite the gate electrode .

77 (original) The transistor of claim 72 wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.

78. (original) The transistor of claim 76 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

79. (original) The transistor of claim 76 wherein the depth of the first source/drain regions is less than the depth of the second source/drain regions.

80. (original) The transistor of claim 76 wherein the second source/drain regions extend into a portion of the substrate.

81. (original) The transistor of claim 76 wherein the first source/drain regions extend into a portion of the substrate.

82. (original) The transistor of claim 72 wherein the substrate is formed of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

83. (original) The transistor of claim 72 wherein the epitaxial layer comprises silicon or silicon germanium.

84. (original) The transistor of claim 72 wherein the gate dielectric layer and gate electrode extend into a trench formed in an upper portion of the substrate.

85. (original) The transistor of claim 84 wherein the trench is of a depth that is less than 50nm.

86. (original) The transistor of claim 72 further comprising a channel region in the substrate under the gate electrode and adjacent the lower side portions of the gate electrode.

87. (original) The transistor of claim 72 wherein the gate dielectric layer comprises a material selected from the group of materials consisting of: silicon oxide film; silicon oxy-nitride (SiON); tantalum oxide; and a high-dielectric-constant material.

88. (original) The transistor of claim 72 wherein the gate dielectric layer is formed using a deposition or thermal oxidation process.

89. (original) The transistor of claim 72 wherein the gate electrode comprises a material selected from the group of materials consisting of polysilicon film; silicon geranium film; silicide film; metal film; and a laminate film.

90. (original) The transistor of claim 72 further comprising a silicon oxide buffer layer between the gate electrode and the insulating spacers.

91. (original) The transistor of claim 72 further comprising a silicide film on the source/drain regions and the gate electrode.

92. (original) The transistor of claim 72, wherein the silicide film comprises a material selected from a group consisting of Co, Ni, W, Ti and combinations thereof.